IN THE CLAIMS

1-24. (Canceled)

25. (Currently Amended) A semiconductor integrated circuit device, comprising:

a memory array having a plurality of word lines, a plurality of bit lines, and a plurality of memory cells;

a processing circuit which carries out an operation using information stored in said memory array; and

an input/output circuit;

wherein said semiconductor integrated circuit device has a first mode and a second mode,

wherein in said first mode ~~said~~a read operation and ~~said~~a write operation to said memory array are performed,

wherein the information stored in said memory array is read out to said input/output circuit in said read operation of said first mode and information outputted from said input/output circuit is written in said memory array in said write operation of the first mode,

wherein in said second mode information stored in said memory array is read from said memory array to said processing circuit,

wherein said processing circuit has an arithmetic unit and a MOS transistor which has a source/drain path between

said arithmetic unit and a power line and a gate inputted with a control signal, and

wherein during said first mode said MOS transistor is in an OFF state.

26. (Previously Presented) The semiconductor integrated circuit device according to claim 25, wherein said

input/output circuit is for inputting and outputting data from and to outside of said semiconductor chip, and

wherein a signal from outside said semiconductor integrated circuit controls whether said semiconductor circuit is in said first mode or said second mode.

27. (Previously Presented) The semiconductor integrated circuit device according to claim 25, further comprising:
a plurality of said memory arrays,

wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and wherein said processing circuit is formed by MOS transistors,

wherein one of said plurality of memory arrays is selected in said first mode, and

wherein said arithmetic unit is placed between two of said plurality of said memory arrays and receives outputs from said two of said plurality of said memory arrays.

28. (Previously Presented) The semiconductor integrated circuit device according to claim 26, wherein each of the plurality of memory cells includes a MOS transistor and a capacitor, and said processing circuit is formed by MOS transistors, and wherein said semiconductor integrated circuit device is formed on a semiconductor chip.

29. (Currently Amended) A semiconductor integrated circuit device on a semiconductor chip, comprising:

a first memory array including a plurality of DRAM memory cells;

a logic circuit carrying out an operation using information stored in said first memory array;

an input/output circuit including latch circuits;

a first bus coupled between said first memory array and said logic circuit;

a second bus coupled between said logic circuit and said input/output circuit; and

a third bus coupled between said first memory array and said input/output circuit,

wherein said semiconductor integrated device has a first mode and a second mode,

wherein in said first mode, by using said third bus, information from outside said semiconductor chip is written to said first memory array or information stored in said first memory array is read out of said semiconductor chip from said first memory array,

wherein in said second mode, by using said first bus, information is read from said first memory array to said logic circuit, by using said second bus, said logic circuit outputs results of said operation to said latch circuit, and by using said third bus, data in accordance with said results is written to said first memory array.

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30. (Previously Presented) The semiconductor integrated circuit device according to claim 29, further comprising:

a second memory array including a plurality of DRAM memory cells,

wherein said logic circuit is placed between said first memory array and said second memory array and receives outputs said first memory array and said second memory array.

31. (Previously Presented) The semiconductor integrated circuit device according to claim 29, further comprising:

a converting circuit which converts said results to said data so that a number of bits used for said data is equal to a

number of bits used for information read out to said logic circuit,

wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor.

32. (Previously Presented) The semiconductor integrated circuit device according to claim 30, wherein each of the plurality of DRAM memory cells includes a MOS transistor and a capacitor.

33. (Previously Presented) The semiconductor integrated circuit device according to claim 30,

wherein mode changing between said first mode and said second mode is performed in accordance with a signal from outside of said semiconductor chip.

34. (Previously Presented) The semiconductor integrated circuit device according to claim 29,

wherein said logic circuit includes an arithmetic unit and a MOS transistor which has a source/drain path between said arithmetic unit and a power line, and

wherein during said first mode said MOS transistor is in off condition.

35. (Previously Presented) The semiconductor integrated circuit device according to claim 29, further comprising:

a comparing circuit comparing said results with an expected value.

36. (Previously Presented) The semiconductor integrated circuit device according to claim 29, further comprising:

a register coupled between said first memory array and said logic circuit,

wherein in said second mode read operation and write operation against said first memory array is performed concurrently.

37. (Previously Presented) The semiconductor integrated circuit device according to claim 29,

wherein said first memory array and said second memory array each further includes sense amplifiers and a precharge circuit.